What is claimed is:

1. A reconfigurable device comprising:

tiles each comprising a circuit; and

an interconnect architecture coupled to the circuit of each tile, the interconnect architecture comprising switches and registers such that in operation some of the switches route a signal from a first tile to a second tile along the interconnect architecture and further such that in operation at least two of the registers consecutively latch the signal at a time interval of no more than a repeating time period.

2. The reconfigurable device of claim 1 wherein the repeating time period comprises a clock cycle period.

3. The reconfigurable device of claim 1 wherein the repeating time period comprises a multiple of a clock cycle period.

4. The reconfigurable device of claim 1 wherein the circuit of one of the tiles comprises elements selected from a group consisting of a look-up table, an arithmetic unit, a multiplier, a reconfigurable interconnect, a memory block, a content addressable memory, a logic element, a specialized functional unit, a logic element, and an other circuit element.

5. The reconfigurable device of claim 1 wherein the tiles comprise heterogeneous tiles.

6. The reconfigurable device of claim 1 wherein the tiles comprise homogeneous tiles.

7. The reconfigurable device of claim 1 wherein the interconnect architecture further comprises data interchanges.

8. The reconfigurable device of claim 7 wherein the data interchanges couple the interconnect architecture to the circuits of the tiles.

9. The reconfigurable device of claim 7 wherein each of the data interchange comprises one of the switches and a plurality of the registers.

10. The reconfigurable device of claim 9 further comprising means for programmatic control at each of the data interchanges.

11. The reconfigurable device of claim 10 wherein the means for programmatic control within each of the data interchanges manages operation of the switches and the registers.

12. The reconfigurable device of claim 9 further comprising means for tag based switching control at each of the data interchanges.

13. The reconfigurable device of claim 12 wherein the means for tag based switching control manages operation of the switches and the registers.

14. The reconfigurable device of claim 13 wherein the means for tag based switching control allows a delay at each of the data interchanges.

15. The reconfigurable device of claim 9 wherein in operation the switch of the data interchange is controlled at least in part by a locally sequenced program.

16. The reconfigurable device of claim 9 wherein in operation the switch of the data interchange is controlled at least in part by a tag comprising a portion of a packet passing through the switch.

17. The reconfigurable device of claim 9 wherein the switch comprises a crossbar switch.

18. The reconfigurable device of claim 9 wherein the switch comprises a statically configured switch.

19. The reconfigurable device of claim 18 wherein the switch further comprises

dynamic switches.

20. The reconfigurable device of claim 7 wherein the data interchange comprises a plurality of the switches.

21. The reconfigurable device of claim 7 wherein the data interchange comprises a register file.

22. The reconfigurable device of claim 7 wherein the interconnect architecture further comprises communication links coupling the data interchanges.

23. The reconfigurable device of claim 22 wherein a length of each of the communication links allows the signal to traverse the communication link within the repeating time period.

24. The reconfigurable device of claim 22 wherein a first communication link couples a first data interchange to a second data interchange.

25. The reconfigurable device of claim 24 wherein a second communication link couples the first data interchange to a third data interchange.

26. The reconfigurable device of claim 24 wherein other communication links couple the first data interchange to other data interchanges.

27. The reconfigurable device of claim 24 wherein other communication links couple the first data interchange to the second data interchange.

28. The reconfigurable device of claim 27 wherein the first communication link and the other communication links comprise a communication channel.

29. The reconfigurable device of claim 1 wherein each tile comprises a mini-tile.

30. The reconfigurable device of claim 1 wherein each tile comprises a plurality of mini-tiles.

31. The reconfigurable device of claim 30 wherein one of the mini-tile comprises a portion of the circuit of one of the tiles.

32. The reconfigurable device of claim 30 wherein each mini-tile couples to the interconnect architecture.

33. The reconfigurable device of claim 32 wherein the interconnect architecture further comprises data interchanges coupling the interconnect architecture to the mini-tiles.

34. The reconfigurable device of claim 33 where each of the data interchanges comprises one of the switches and a plurality of the registers.

35. The reconfigurable device of claim 34 wherein the data interchanges further comprises bypasses.

36. A reconfigurable device comprising:

tiles each comprising a circuit and a tile size such that in operation the tile size allows a first signal to traverse the circuit within about a repeating time period; and

an interconnect architecture coupled to the circuit of each tile, the interconnect architecture comprising switches and registers such that in operation some of the switches route a second signal from a first tile to a second tile along the interconnect architecture and further such that in operation at least two of the registers consecutively latch the second signal at a time interval of no more than the repeating time period.

37. The reconfigurable device of claim 36 wherein the repeating time period comprises a clock cycle period.

38. The reconfigurable device of claim 36 wherein the repeating time period comprises a multiple of a clock cycle period.

39. A reconfigurable device comprising:

tiles each comprising a circuit; and

an interconnect architecture coupled to the circuit of each tile, the interconnect architecture comprising switches and registers such that in operation some of the switches route a signal from a first tile to a second tile along the interconnect architecture and further such that in operation at least two of the registers latch the signal at a time interval of no more than a clock cycle period.

40. A reconfigurable device comprising:

first, second, and third tiles each comprising a circuit; and

an interconnect architecture comprising first, second, and third data interchanges and first and second data transport segments, wherein:

the first, second, and third data interchanges couple the interconnect architecture to the circuits of the first, second, and third tiles, respectively;

the first and second data transport segments couple the first data interchange to the second and third data interchanges, respectively; and

the first, second, and third data interchanges each comprise a switch and registers such that in operation two of the switches route a signal from the first tile to the second tile via the first data transport segment and further such that in operation one of the registers of the second data interchange latches the signal prior to the signal entering the circuit of the second tile.

41. A reconfigurable device comprising:

first, second, and third tiles each comprising a circuit; and

an interconnect architecture comprising first, second, and third data interchanges and first and second data transport segments, wherein:

the first, second, and third data interchanges couple the interconnect architecture to the circuits of the first, second, and third tiles, respectively;

the first and second data transport segments couple the first

data interchange to the second and third data interchanges, respectively; and

the first, second, and third data interchanges each comprise a switch and registers such that in operation the switches of the first and second data interchanges route a signal from the first tile to the second tile via the first data transport segment and further such that in operation one of the registers of the first data interchange latches the signal at a first time and one of the registers of the second data interchange latches the signal at a later time within no more than a clock cycle period of the first time.